REMARKS

This application has been carefully reviewed in light of the Office Action dated June 22, 2009. Claims 1 to 12, 14 to 22 and 24 are pending in the application, with Claims 13 and 23 having been cancelled herein without prejudice or disclaimer of subject matter. Claims 1, 7 to 10 and 18 to 22 are in independent form. Reconsideration and further examination are respectfully requested.

Claims 1, 8, 9, 18, 20 and 21 were objected to because of an informality. The objections are believed to be obviated by the foregoing amendments to the claims, and reconsideration and withdrawal of the objections are respectfully requested.

Claims 1 to 24 were rejected under 35 U.S.C. § 102(b) over "Hierarchical Pulse-coupled Neural Network Model with Temporal Coding and Emergent Feature Binding Mechanism", 2001 (Matsugu). Reconsideration and withdrawal of the rejections are respectfully requested.

The claims are directed to parallel pulse signal processing apparatuses and control methods therefor. Among many other features, the claims include a feature of a gate circuit which counts pulse signals corresponding to predetermined upper output levels, and passes the pulse signals corresponding to the predetermined upper output levels until a number of the counted pulse signals reaches a predetermined number.

Referring specifically to claim language, amended independent Claim 1 is directed to a parallel pulse signal processing apparatus. The apparatus includes a plurality of pulse output arithmetic elements, a plurality of connection elements which connect predetermined elements of the arithmetic elements in parallel, and a gate circuit which selectively passes pulse signals received from the plurality of connection elements. The

pulse output arithmetic elements include input means for inputting a plurality of time series pulse signals, modulation processing means for executing predetermined modulation processing on a basis of the input plurality of time series pulse signals, and pulse output means for outputting a pulse signal on a basis of a result of the modulation processing. The gate circuit counts, of the pulse signals output from the plurality of pulse output arithmetic elements and received from the plurality of connection elements, pulse signals corresponding to predetermined upper output levels, and passes the pulse signals corresponding to the predetermined upper output levels until a number of the counted pulse signals reaches a predetermined number.

Amended independent Claim 7 is directed to a parallel pulse signal processing apparatus which hierarchically executes a plurality of arithmetic processing operations. The apparatus includes a plurality of arithmetic elements which receives signals from different layer levels and outputs predetermined pulse signals by a predetermined local receptor field structure. The apparatus further includes a gate circuit element which counts, of the pulse signals output from the plurality of arithmetic elements belonging to a predetermined receptor field, pulse signals corresponding to predetermined upper output levels, and passes the pulse signals corresponding to the predetermined upper output levels until a number of the counted pulse signals reaches a predetermined number.

Amended independent Claim 8 is directed to a parallel pulse signal processing apparatus. The apparatus includes input means for inputting data in a predetermined dimension, a plurality of data processing means, a gate circuit which selectively passes pulse signals from the data processing means, and output means for outputting a result of pattern detection. The data processing means includes a plurality of

arithmetic elements connected by predetermined connection means in parallel. The arithmetic elements included in the data processing means output a pulse shaped signal train representing a detection result of a pattern of a predetermined category on a basis of an arrival time pattern of a plurality of pulses from predetermined arithmetic elements input in a predetermined time window. The gate circuit counts, of pulse signals included in the pulse shaped signal train output from the plurality of arithmetic elements and received from the plurality of connection elements, pulse signals corresponding to predetermined upper output levels, and passes the pulse signals corresponding to the predetermined upper output levels until a number of the counted pulse signals reaches a predetermined number. The output means outputs the detection result of the predetermined pattern in the data on a basis of the outputs from the arithmetic elements.

Amended independent Claim 9 is directed to a parallel pulse signal processing apparatus. The apparatus includes input means for inputting data in a predetermined dimension, a plurality of data processing means for outputting pulse signals, a gate circuit which selectively passes pulse signals output and received from the data processing means, and output means for outputting a result of pattern detection. The data processing means includes a plurality of arithmetic elements connected by predetermined connection means in parallel. The gate circuit counts, of the pulse signals output and received from the plurality of data processing means, pulse signals corresponding to predetermined upper output levels, and passes the pulse signals corresponding to the predetermined upper output levels until a number of the counted pulse signals reaches a predetermined number. The arithmetic elements receive a time series pulse signal, identify time series pulse signal patterns of a plurality of classes, and output a pulse shaped signal

train unique to an arrival time pattern of a plurality of predetermined pulse signals input in a predetermined time window. The output means outputs the detection result of a predetermined pattern in the data on the basis of the outputs from the arithmetic elements.

Amended independent Claim 10 is directed to a parallel pulse signal processing apparatus which hierarchically executes a plurality of arithmetic processing operations. The apparatus includes input means for inputting one of an intermediate result of different layer levels and data from a predetermined memory, a plurality of data processing means, having a feature detection layer which detects a plurality of features from the data input by the input means, for outputting pulse signals, and a timing signal generation circuit. The plurality of data processing means further includes a plurality of arithmetic elements which receives detection signals of the features of different types from a layer level of a preceding stage and outputs predetermined pulse signals. The plurality of data processing also includes a gate circuit which counts, of the pulse signals output from the arithmetic elements involved in the plurality of predetermined features, pulse signals corresponding to predetermined upper output levels, and passes the pulse signals corresponding to the predetermined upper output levels until a number of the counted pulse signals reaches a predetermined number. The arithmetic elements output the pulse signals at one of a frequency and a timing based on a plurality of input signals from the timing signal generation circuit and an arrival time pattern of a plurality of pulses in a predetermined time window.

Amended independent Claims 18 to 22 are directed to method claims substantially corresponding to apparatus Claims 1 and 7 to 10, respectively.

The applied reference of Matsugu is not seen to disclose or suggest all of the features of Claims 1, 7 to 10 and 18 to 22, and in particular, is not seen to disclose or suggest at least the features of counting by a gate circuit, of pulse signals output from a plurality of pulse output arithmetic elements and received from a plurality of connection elements (Claims 1 and 18), or of pulse signals output from a plurality of arithmetic elements belonging to a predetermined receptor field (Claims 7 and 19), or of pulse signals included in a pulse shaped signal train output from a plurality of arithmetic elements and received from a plurality of connection elements (Claims 8 and 20), or of pulse signals output and received from a plurality of data processing means (Claims 9 and 21), or of pulse signals output from arithmetic elements involved in a plurality of predetermined features (Claims 10 and 22), pulse signals corresponding to predetermined upper output levels, and passing by the gate circuit the pulse signals corresponding to the predetermined upper output levels until a number of the counted pulse signals reaches a predetermined number.

In this regard, Matsugu is seen to disclose a pulse phase modulation system, in which each neuron in a feature detection layer is coupled by pulse phase modulating synapses which are connected with a local bus line. A gating neuron is also connected with a local timing neuron to the local bus line. Local timing inter-neurons are introduced in-between a feature pooling and a detecting layer to embed a distributed timing mechanism in the system. Pulse signals are controlled by the gating neuron which opens the local bus line over some duration. (See pages 802 and 803 of Matsugu). Thus, the gating neuron of Matsugu is merely seen to pass the pulse signals during a certain period of time. In contrast, in Claims 1, 7 to 10 and 18 to 22, a gate circuit passes pulse signals corresponding

to predetermined upper output levels until a number of pulse signals corresponding to the predetermined upper output levels counted by the gate circuit reaches a predetermined number.

Therefore, Matsugu is not seen to disclose or suggest counting by a gate circuit, of pulse signals output from a plurality of pulse output arithmetic elements and received from a plurality of connection elements (Claims 1 and 18), or of pulse signals output from a plurality of arithmetic elements belonging to a predetermined receptor field (Claims 7 and 19), or of pulse signals included in a pulse shaped signal train output from a plurality of arithmetic elements and received from a plurality of connection elements (Claims 8 and 20), or of pulse signals output and received from a plurality of data processing means (Claims 9 and 21), or of pulse signals output from arithmetic elements involved in a plurality of predetermined features (Claims 10 and 22), pulse signals corresponding to predetermined upper output levels, and passing by the gate circuit the pulse signals corresponding to the predetermined upper output levels until a number of the counted pulse signals reaches a predetermined number.

Accordingly, Claims 1, 7 to 10 and 18 to 22 are believed to be in condition for allowance, and such action is respectfully requested.

The other claims in the application are each dependent from the independent claims discussed above and are therefore believed to be allowable over the applied references for at least the same reasons. Because each dependent claim is deemed to define an additional aspect of the invention, however, the individual consideration of each on its own merits is respectfully requested.

No other matters being raised, it is believed that the entire application is fully in condition for allowance, and such action is courteously solicited.

Applicant's undersigned attorney may be reached in our Costa Mesa, California office at (714) 540-8700. All correspondence should continue to be directed to our below-listed address.

Respectfully submitted,

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